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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/628,578 | 07/29/2003 | Antoni Fertner | 1410-794 | 4094 |

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| EXAMINER | |
|---|---|
| PHAN, THAI Q | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2128 | |

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/628,578 | FERTNER ET AL. | |
| | Examiner | Art Unit | |
| | Thai Q. Phan | 2128 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This Office Action is in response to patent application S/N: 10/628,578. Claims 1-40 are pending in the action.

### *Drawings*

The drawings filed on 07/29/2003 are acceptable for examination.

### *Specification*

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

### *Claim Objections*

Claim 2 is objected to because of the following informalities: the claim is ended with double dot. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Gopal, Nanda, US patent no. 6,134,513.

As per claim 1, Gopal anticipates a method and system including computer program product for simulating a large, hierarchical resistive network with feature limitations very identical to the claimed invention. According to Gopal, the method includes:

Generating an admittance matrix for an electrical which is being analyzed, the admittance matrix including symbolic expressions for at least some circuit components of the electric circuit (col. 5, lines 55-65, col. 9, line 50 to col. 10, line 40),

And linearly and algebraically solving an equation system including the admittance matrix for analyzing at least a part of the electric circuit (Figs. 15 and 16, cols. 9 and 10).

As per claims 2-3, Gopal anticipates the system is to solve for network transfer function and resistive network components as claimed.

As per claim 4, Gopal anticipates the admittance matrix for a plurality of circuit components or subcircuits (Figs. 15).

As per claim 5, Gopal anticipates the admittance blocks for the plural subcircuits are parsed or situated on a main diagonal of the admittance matrix (Figs. 15 and 16), and the admittance matrix is symmetrical (Fig. 16, col. 10, lines 41-68).

As per claims 6 and 7, Gopal anticipates circuit cut node analysis with limitations as claimed.

As per claim 8, Gopal anticipates a method and system including computer program product for simulating a large, hierarchical resistive network with feature limitations very identical to the claimed invention. According to Gopal, the computation method includes:

Generating an admittance matrix for an electrical which is being analyzed, the admittance matrix including symbolic expressions for at least some circuit components of the electric circuit (col. 5, lines 55-65, col. 9, line 50 to col. 10, line 40),

And linearly and algebraically solving an equation system including the admittance matrix for analyzing at least a part of the electric circuit (Figs. 15 and 16, cols. 9 and 10).

As per claims 9-10, Gopal anticipates the system is to solve for network transfer function and resistive network components as claimed.

As per claim 11, Gopal anticipates the admittance matrix for a plurality of circuit components or subcircuits (Figs. 15).

As per claim 12, Gopal anticipates the admittance blocks for the plural subcircuits are parsed or situated on a main diagonal of the admittance matrix (Figs. 15 and 16), and the admittance matrix is symmetrical (Fig. 16, col. 10, lines 41-68).

As per claims 13-14, Gopal anticipates circuit cut node analysis with limitations as claimed.

As per claim 15, Gopal anticipates a computer program product for simulating a large, hierarchical resistive network with feature limitations very identical to the claimed invention. According to Gopal, program product includes means:

Generating an admittance matrix for an electrical which is being analyzed, the admittance matrix including main circuit admittance blocks for main circuit, subcircuit admittance blocks for subcircuits, block connectivities, symbolic expressions for at least some circuit components of the electric circuit (col. 5, lines 55-65, col. 9, line 50 to col. 10, line 40),

And linearly and algebraically solving an equation system including the admittance matrix for analyzing at least a part of the electric circuit (Figs. 15 and 16, cols. 9 and 10).

As per claims 16-17, Gopal anticipates the system is to solve for network transfer function such as node voltage or node currents, and resistive network components as claimed.

As per claims 18 and 19, Gopal anticipates the network transfer function, node voltage, node current, etc. for a plurality of circuit components or subcircuits (Figs. 15).

As per claim 20, Gopal anticipates the admittance blocks for the plural subcircuits such as filter, circuit transformers, etc. as claimed (Figs. 15 and 16), and the admittance matrix is symmetrical (Figs. 5, 16, col. 5, lines 56-65, col. 10, lines 41-68).

As per claim 21, Gopal anticipates a method and system including computer program product for simulating a large, hierarchical resistive network with feature limitations very identical to the claimed invention. According to Gopal, the method includes:

Generating an admittance matrix for an electrical which is being analyzed, the admittance matrix including symbolic expressions rather than numerical expression for

at least some circuit components of the electric circuit (col. 5, lines 55-65, col. 9, line 50 to col. 10, line 40),

And linearly and algebraically solving an equation system including the admittance matrix for analyzing at least a part of the electric circuit (Figs. 15 and 16, cols. 9 and 10).

As per claims 22-23, Gopal anticipates the system is to solve for network transfer function and resistive network components as claimed.

As per claim 24, Gopal anticipates the admittance matrix for a plurality of circuit components or subcircuits (Figs. 15).

As per claim 25, Gopal anticipates the admittance blocks for the plural subcircuits are parsed or situated on a main diagonal of the admittance matrix (Figs. 15 and 16), and the admittance matrix is symmetrical (Fig. 16, col. 10, lines 41-68).

As per claims 26-27, Gopal anticipates circuit cut node analysis with limitations of nodal analysis, node rearrangement, simplifying node equations, node equations, node transfer functions, etc. as claimed.

As per claim 28, Gopal anticipates a method and system including computer program product for simulating a large, hierarchical resistive network with feature limitations very identical to the claimed invention. According to Gopal, the method includes:

Generating an admittance matrix for an electrical which is being analyzed, the admittance matrix including symbolic expressions for at least some circuit components

of the electric circuit rather than numerical expression in the nodal analysis (col. 5, lines 55-65, col. 9, line 50 to col. 10, line 40),

And linearly and algebraically solving an equation system including the admittance matrix for analyzing at least a part of the electric circuit (Figs. 15 and 16, cols. 9 and 10).

As per claims 29-30, Gopal anticipates the system is to solve for network transfer function, sensitivity analysis, circuit optimization, and resistive network components as claimed.

As per claim 31, Gopal anticipates the admittance matrix for a plurality of circuit components or subcircuits (Figs. 15).

As per claim 32, Gopal anticipates the admittance blocks for the plural subcircuits are parsed or situated on a main diagonal of the admittance matrix (Figs. 15 and 16), and the admittance matrix is symmetrical (Fig. 16, col. 10, lines 41-68).

As per claims 33-34, Gopal anticipates circuit cut node analysis with limitations as claimed.

As per claim 35, Gopal anticipates a method and computer program product implemented in a simulation system for simulating a large, hierarchical resistive network with feature limitations very identical to the claimed invention. According to Gopal, the simulation method includes:

Generating an admittance matrix for an electrical which is being analyzed, the admittance matrix including main circuit admittance blocks for main circuit, subcircuit admittance blocks for subcircuits, block connectivities, symbolic expressions for at least

some circuit components of the electric circuit (col. 5, lines 55-65, col. 9, line 50 to col. 10, line 40),

And linearly and algebraically solving an equation system including the admittance matrix for analyzing at least a part of the electric circuit (Figs. 15 and 16, cols. 9 and 10).

As per claims 36-37, Gopal anticipates the system is to solve for network transfer function such as node voltage or node currents, and resistive network components as claimed.

As per claims 38 and 39, Gopal anticipates the network transfer function, node voltage, node current, etc. for a plurality of circuit components or subcircuits (Figs. 15).

As per claim 40, Gopal anticipates the admittance blocks for the plural subcircuits such as filter, circuit transformers, etc. as claimed (Figs. 15 and 16), and the admittance matrix is symmetrical (Figs. 5, 16, col. 5, lines 56-65, col. 10, lines 41-68).

***Conclusion***

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 5,313,398, issued to Rohrer et al, on May 1994
2. US patent no. 5,629,845, issued to Liniger, Werner, on May 1997
3. US patent no. 5,692,158, issued to Degeneff et al, on Nov. 1997
4. US patent no. 6,807,520 B1, issued to Zhou et al, on Oct. 2004
5. US patent application publication no. US 2003/0065498 A1, issued to Bois et al.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Thai Phan whose telephone number is 571-272-3783.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on 571-272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Apr. 29, 2005

Thai Phan
Patent Examiner